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**INFORMATION DISCLOSURE  
STATEMENT**

**BY APPLICANT**

Docket: 1011-54375

App: 09/620,021

Applicant: Rajski et al.

Filed: July 20, 2000

Art Unit: ~~2858~~ 2133

**U.S. PATENT DOCUMENTS**

Init.*	Number	Date	Name	Class	Sub	Filed
PMC	3,614,400	Oct-71	Farnett	1	1	
	3,700,869	Oct-72	Low et al.	1	1	
	4,503,537	Mar-85	McAnney	1	1	
	4,687,988	Aug-87	Eichelberger et al.	1	1	
	4,754,215	Jun-98	Kawai	1	1	
	4,785,410	Nov-88	Hamatsu et al.	1	1	
	4,801,870	Jan-89	Eichelberger et al.	1	1	
	4,860,236	Aug-89	McLeod et al.	1	1	
	4,959,832	Sep-90	Bardell, Jr.	1	1	
	4,974,184	Nov-98	Avra	1	1	
	5,090,035	Feb-92	Murase	1	1	
	5,138,619	08/11/92	Fasang et al.	1	1	
	5,173,906	12/22/1992	Dreibelbis et al.	1	1	
	5,268,949	Dec-93	Watanabe	1	1	
	5,301,199	04/05/1994	Ikenaga et al.	1	1	
	5,325,367	Jun-94	Dekker et al.	1	1	
PMC	5,369,648	Nov-94	Nelson	1	1	

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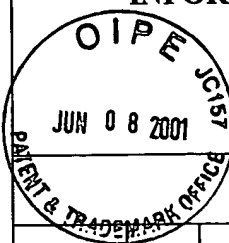
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**U.S. PATENT DOCUMENTS**

Init.*	Number	Date	Name	Class	Sub	Filed
<i>me</i>	5,394,405	Feb-95	Savir	—	—	
	5,412,665	May-95	Gruodis et al.	—	—	
	5,414,716	May-95	Bershteyn	—	—	
	5,446,683	Aug-95	Mullen et al.	—	—	
	5,450,414	Sep-95	Lin	—	—	
	5,574,733	Nov-96	Kim	—	—	
	5,586,125	12/17/1996	Warner	—	—	
	5,612,963	Mar-97	Koenemann et al.	—	—	
	5,631,913	May-97	Maeda	—	—	
	5,694,402	12/02/1997	Butler et al.	—	—	
	5,719,913	Feb-98	Maeno	—	—	
	5,748,497	May-98	Scott et al.	—	—	
	5,790,562	08/04/98	Murray et al.	—	—	
	5,790,626	Aug-98	Johnson et al	—	—	
	5,831,992	Nov-98	Wu	—	—	
	5,899,961	May-99	Sundermann	—	—	
<i>PC</i>	5,974,433	Oct-99	Currie	—	—	

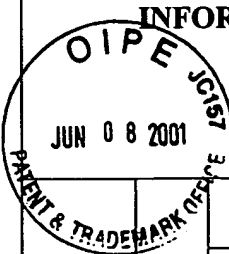
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**U.S. PATENT DOCUMENTS**

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<b>INFORMATION DISCLOSURE STATEMENT</b> <b>BY APPLICANT</b>		Docket: 1011-54375	App: 09/620,021
		Applicant: Rajski et al.	
		Filed: July 20, 2000	Art Unit: 2858
 pme		J. Rajski, J. Tyszer, N. Zacharia, "Test Data Decompression for Multiple Scan Designs with Boundary Scan," IEEE Transactions on Computers, Vol. 47, No. 11, November 1998	
		J. Rajski and J. Tyszer, "Design of Phase Shifters for BIST Applications", <i>Proc. VLSI Test Symposium</i> , pp. 218-224, 1998.	
		J. Rajski, N. Tamarapalli, J. Tyszer, "Automated Synthesis of Large Phase Shifters for Built-In Self-Test," International Test Conference, Paper 41.1, pp. 1047-1056, IEEE 1998	
		Venkataraman, Rajski, Hellebrand, and Tarnick, "An Efficient BIST Scheme Based on Reseeding of Multiple Polynomial Linear Feedback Shift Registers", pp. 572-577, 1993 IEEE	

## U.S. PATENT APPLICATION DOCUMENTS

Init.*	Application Number	Filing Date	Name	Class	Sub	Filed
	<del>09/713,662</del>	<del>11/15/2000</del>	<del>Rajski et al.</del>			
	<del>09/713,664</del>	<del>11/15/2000</del>	<del>Rajski et al.</del>			
	<del>09/619,988</del>	<del>07/20/2000</del>	<del>Rajski et al.</del>			
	<del>09/620,023</del>	<del>07/20/2000</del>	<del>Rajski et al.</del>			
	<del>09/619,985</del>	<del>07/20/2000</del>	<del>Rajski et al.</del>			

Note: These US patent applications had not been considered by Examiner because the US patent applications can't be (considered) listed as Prior Art for a suggestion these copending US patent applications should be listed in the specification.

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Docket: 1011-54375

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Applicant: Rajski et al.

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Art Unit: ~~288~~ 2133

	Number	Date	Name	Class	Sub	Filed
pmc	5,991,898	11/23/1999	Rajski et al.			
	5,991,909	11/23/1999	Rajski et al.			
	6,006,349	Dec-99	Fujisaki			
	6,072,823	Jun-00	Takakusaki			
pmc	6,141,669	Oct-00	Carleton			

## OTHER DOCUMENTS

pmc		P.H. Bardell, "Design Considerations for Parallel Pseudorandom Pattern Generators", Journal of Electronic Testing: Theory and Applications, 1,73-87 (1990)
pmc		I. Hamzaoglu, J. Patel, "Reducing Test Application Time for Full Scan Embedded Cores," Center for Reliable & High-Performance Computing, University of Illinois, Urbana, IL., 1999 IEEE
pmc		S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman, B. Courtois, "Built-in Test for Circuits With Scan Based on Reseeding of Multiple Polynomial Linear Feedback Shift Registers", <i>IEEE Trans. On Computers</i> , vol. C-44, pp. 223-233, 1995.
pmc		S. Hellebrand, B. Reeb, S. Tarnick, H-J Wunderlich, "Pattern Generation for a Deterministic BIST Scheme", pp. 88-94 1995 IEEE
pmc		B. Koenemann c/o IBM Corp., B56/901, "LFSR-Coded Test Patterns for Scan Designs", <i>Proceedings of European Test Conference</i> , pp. 237-242, 1991.

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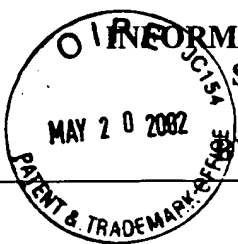
pmc		J. Rajski, J. Tyszer, N. Zacharia, "Decompression of Test Data Using Variable-Length Seed LFSRs" Microelectronics and Computer Systems Laboratory, McGill University, Montreal, Canada, 1995 IEEE
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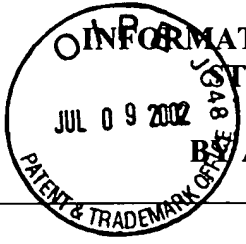
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				Applicant: Rajski et al.			
				Filed: July 20, 2000		Art Unit: <del>2058</del> 2133	
<b>U.S. PATENT DOCUMENTS</b>							
Init.*		Number	Date	Name	Class	Sub	Filed
pmc		4,513,418	4/1985	Bardell, Jr. et al.			
		4,602,210	7/1986	Fasang et al.			
		5,905,986	5/1999	Rohrbaugh et al.			
		5,592,493	1/1997	Crouch et al.			
		6,158,032	12/2000	Currier et al.			
pmc		6,300,885	10/2001	Davenport et al.			
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		Docket: 1011-54375	App: 09/620,021
		Applicant: Rajski et al.	
		Filed: July 20, 2000	Art Unit: <del>2858</del> 2/33
<b>OTHER DOCUMENTS</b>			
me			Bershteyn, M., "Calculation of Multiple Sets of Weights for Weighted Random Testing," International Test Conference 1993, Paper 45.3, pp. 1031-1040.
me			Zacharia, N. et al, "Decompression of Test Data Using Variable-Length Seed LFSRs," IEEE 1995, 426-433.
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<b>U.S. PATENT DOCUMENTS</b>							
Init.*		Number	Date	Name	Class	Sub	Filed
Pmc		6,385,750	May, 2002	Kapur et al.			
<b>FOREIGN PATENT DOCUMENTS</b>							
		Number	Date	Country	Class	Sub	
<b>OTHER DOCUMENTS</b>							
Pmc			Mano, M. Morris, "Computer System Architectures," 2 <sup>nd</sup> Edition, Prentice-Hall, Inc., New Jersey, 1982.				
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